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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,449	10/29/2003	Guy Cohen	P-5484-US	4557

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,449	COHEN ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-12 and 14-19* is/are rejected.

7)☒ Claim(s) *7-9 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on October 29, 2003 and the Information Disclosure Statement filed on December 13, 2004.

2. Claims 1 – 19 are pending in this case. Claims 1, 15, 18, and 19 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 6, 10 – 12 and 15 – 19, are rejected under 35 U.S.C. 102(b) as being anticipated by Mi et al. U.S. Patent No. 5,608,679.

Regarding independent claim 1, Fig. 7 of Mi et al. discloses a multi-phase method of programming an array of non-volatile memory cells (Fig. 2 [20]), said method comprising: applying to a first set of NVM cells first phase programming pulses (Fig. 7 [One program pulse]; and Col. 9 lines 36 – 39), and upon one or more NVM cells of the first set of cells reaching or exceeding a first intermediate threshold voltage level (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56), applying to a terminal of one or more cells in the first set of cells second phase programming pulses (Fig. 7 [pulse width = P3 One program pulse]; and Col. 9 lines 57 – 61) adapted to induce relatively greater

threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge (Col. 9 lines 64 - 67).

Regarding dependent claim 2, Mi et al. discloses wherein applying first phase programming pulses (Fig. 7 [One program Pulse]) to one or more NVM cells of the first set of cells of one or more NVM cells of the first comprises applying to a terminal set of NVM cells incrementally increasing programming pulses in concert with pulses of substantially fixed voltage applied to gates of the one or more NVM cells (Col. 9 lines 1 – 12, and Col. 9 lines 43 – 52); and wherein applying second phase programming pulses (Fig. 7 [Pulse width=3 One program pulse]), comprises applying to a terminal of the one or more cells (Col. 9 lines 58 60) programming pulses of substantially fixed voltage in concert with gate pulse of incrementally increasing voltage (Col. 9 lines 64 – 67).

Regarding dependent claim 3, Mi et al. discloses wherein applying to a terminals of the one or more cells of the first set second phase programming pulses of substantially fixed voltage in concert with gate pulse of incrementally increasing voltage is repeated until one or more of the cells of the first set reaches a first target threshold voltage level (See Fig. 7 for repeating steps until cells memory has reached the target level).

Regarding dependent claim 4, Mi et al. discloses wherein the second phase programming pulses of substantially fixed voltage (Fig. 7 Pulse width = P3 One program pulse]) are at a voltage corresponding to the voltage of the programming pulse which first succeeded in raising the threshold voltage (Fig. 7 [Vt]) of one or more cells of said

first set to or beyond the first intermediate threshold voltage (Fig 7 [Vt >= secondary target 'yes']).

Regarding dependent claim 5, Mi et al. discloses wherein the initial value of the second phase gate pulses are at a voltage (Fig. 7 Pulse width = P3 One program pulse]) corresponding to the gate voltage of the programming pulse which first succeeded in raising the threshold voltage (Fig. 7 [Vt]) of one or more cells of said first set to or beyond the first intermediate threshold voltage (Fig 7 [Vt >= secondary target 'yes']).

Regarding dependent claim 6, Mi et al. discloses wherein the NVM cell is a multi-level cell (Fig.7 disclosing multilevel programming for memory cells)

Regarding dependent claim 10, Mi et al. discloses wherein first phase programming (Fig. 7 [One program Pulse]) comprises applying to a terminal of one or more NVM cells of a first set of NVM cells (Col. 9 lines 36 – 42) incrementally increasing programming pulses in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells (Col. 9 lines 43 – 52), and wherein applying second phase programming pulses (Fig. 7 [Pulse width = P3 One program pulse]) to one or more cells in the first set comprises applying to a terminal (Col. 9 lines 57 – 60) of the one or more cells programming pulses of incrementally increasing voltage in concert with gates pulses of a relatively reduced and substantially fixed voltage (Col. 9 lines 61 – 67).

Regarding dependent claim 11, Mi et al. discloses wherein applying to a terminal of one or more cells of a first set programming pulses of incrementally increasing voltage is repeated until all of the one or more cells of said first set reaches a

first target threshold voltage (See Fig. 7 for repeating steps until memory cells have charged reached the target level).

Regarding dependent claim 12, Mi et al. discloses wherein the NVM cell is a multi-level cell (Fig.7 disclosing multilevel programming for memory cells).

Regarding independent claim 15, Fig. 4 of Mi et al. discloses a System for programming an array of non-volatile memory ("NVM") cells, said system comprising; a controller (Fig. 4 [Controller] adapted to cause a charge circuit (Fig. 7) to produce first phase programming (Fig. 7 [One Program pulse]) and to determine when one or more NVM cell of a first set of cells receiving the first phase programming pulses (Col. 9 lines 37 – 42) reaches or exceeds a first intermediate voltage (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56), and to then cause said charge pump circuit to apply to a terminal the one or more cells in the first set second phase programming pulses (Fig. 7 [pulse width = P3 One program pulse]; and Col. 9 lines 57 – 61) adapted to induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge (Col. 9 lines 64 - 67).

Regarding dependent claim 16, Mi et al. discloses wherein said controller (Fig. 4 [Controller]) is adapted to cause said charge pump circuit (Fig. 7) to initially apply to a terminal of one more NVM cells of the first set of NVM cells first phase programming pulses having incrementally increasing voltage levels in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells (Col. 9 lines 1 – 12, and Col. 9 lines 43 – 52), and once the threshold voltage of a one or more cells reaches or exceeds an intermediate threshold voltage level (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56), said controller (Fig. 4 [Controller]) adapted to

cause said charge pump circuit (Fig. 7) to apply to a terminal of one or more cells second phase programming pulses (Fig. 7 [Pulse width = P3 One program pulse]) of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage (Fig. 7).

Regarding dependent claim 17, Mi et al. discloses wherein said controller (Fig. 4 [Controller]) is adapted to cause said charge pump circuit (Fig. 7) to initially apply to a terminal of one or more NVM cells of the first set of NVM cells first phase programming pulses of incrementally increasing voltage in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells (Col. 9 lines 1 – 12, and Col. 9 lines 43 – 52), and once the threshold voltage of one or more cells reaches or exceeds an intermediate threshold voltage level (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56) said controller (Fig. 4 [Controller]) adapted to cause said charge pump circuit (Fig. 7) to apply to a terminal of one or more cells second phase programming pulses (Fig. 7 [Pulse width = P3 One program pulse]) of incrementally increasing voltage (Fig. 7) in concert with gate pulses (Fig. 4) of substantially fixed and reduced voltage (Fig. 7 [Vt>= Target]).

Regarding independent claim 18, Fig. 7 of Mi et al. discloses a multi-phase method of programming an array of non-volatile memory cells (Fig. 1 [16]), said method comprising: applying to a first set of NVM celli first phase programming pulses (Fig. 7 [One program pulse]; and Col. 9 lines 36 – 39); and upon one or more NVM cells of the first set of cells reaching or exceeding a first intermediate threshold voltage level (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56), applying to a terminal of one or more cells in the first set of cells second phase programming pulses (Fig. 7 [pulse width

= P3 One program pulse]; and Col. 9 lines 57 – 61) adapted to induce deterministically lower programming rate for all cells in first set (Fig. 7 [Vt>= Target]).

Regarding independent claim 19, Fig. 4 of Mi et al. discloses a System for programming (Fig. 7) an array of non-volatile memory (Fig. 7 [16]) cells, said system comprising: a controller (Fig. 4 [controller]) adapted to cause a charge circuit (Fig. 7) to produce first phase programming pulses (Fig. 7 [One program pulse]) and to determine when one or more NVM cell of a first set of cells receiving the first phase programming pulses (Col. 9 lines 37 – 42) reaches or exceeds a first intermediate voltage (Fig. 7 [Vt >= secondary target 'Yes']; and Col. 9 lines 53 – 56), and to then cause said charge circuit to apply to a terminal of the one or more cells in the first set second phase programming pulses (Fig. 7 [pulse width = P3 One program pulse]; and Col. 9 lines 57 – 61) adapted to induce a deterministically reduced programming rate (Fig. 7 [Vt>= Target]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mi et al. U.S. Patent No. 5,608,679 in view of Applicant Admitted Prior Art (AAPA).

Mi et al. as applied to claim 1 above, fails to disclose the NVM cell is selected from the group consisting of Nitride Read Only Memory ("NROM"), multi-level cell (MLC), dual charge trapping region NROM, and dual charge trapping region MLC NROM.

Fig. 2B and on page 1, under Background, AAPA discloses non-volatile memory is selected from a group consisting of Nitride Read Only Memory (AAPA, page 1, lines 13 – 15).

Mi et al. and AAPA are common subject matter for nonvolatile memory device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to fabricate the nonvolatile memory of Mi et al. by Nitride Read Only Memory taught by AAPA, since Nitride Read Only Memory is a well known and conventional device for nonvolatile memory as has indicated by AAPA, therefore selected a known memory material on the basis of its suitability for in intended of use as a matter of obvious material of interests.

Allowable Subject Matter

5. Claims 7 – 9, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 7 and 13, in addition to other elements in each respective claim, the prior art fails to teach or suggests "applying to a terminal of one or more NVM cells of a second set of NVM cells to be programmed to a second target threshold voltage".

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jeong	Patent No. US 6,353,555 B1	Date of Patent: Mar. 5, 2002
Chen	Patent No. US 6,456,528 B1	Date of Patent: Sep. 24, 2002

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 2/28/2005

VAN THU NGUYEN
PRIMARY EXAMINER